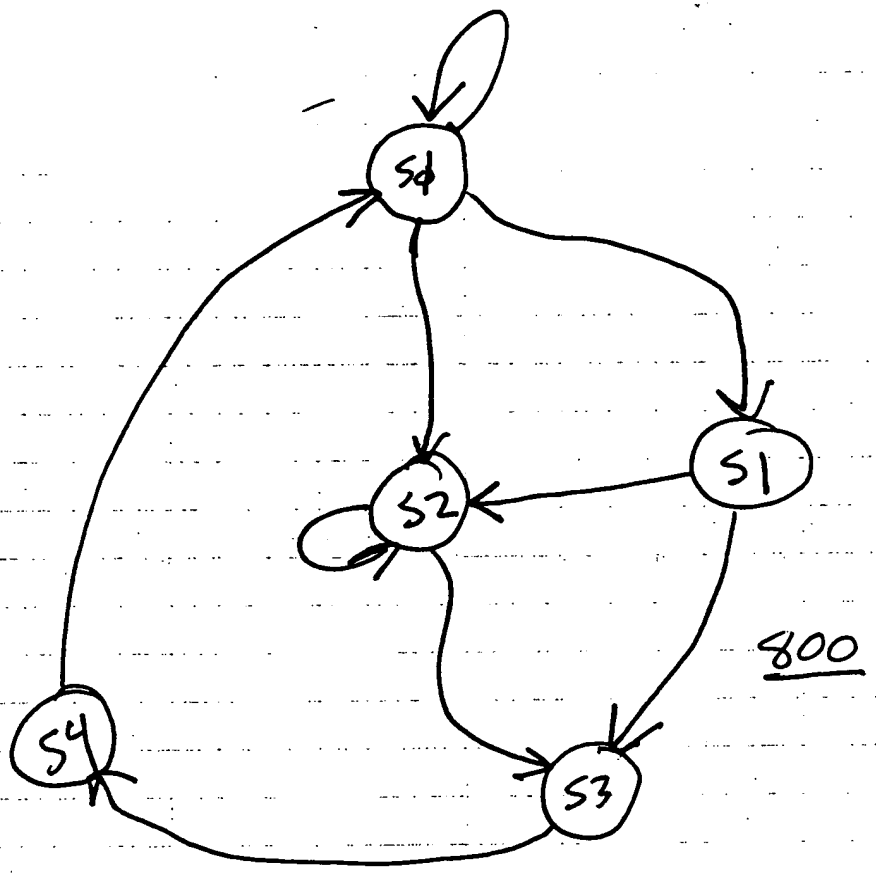




FIG. 8A (Amended)

(Prior Art)

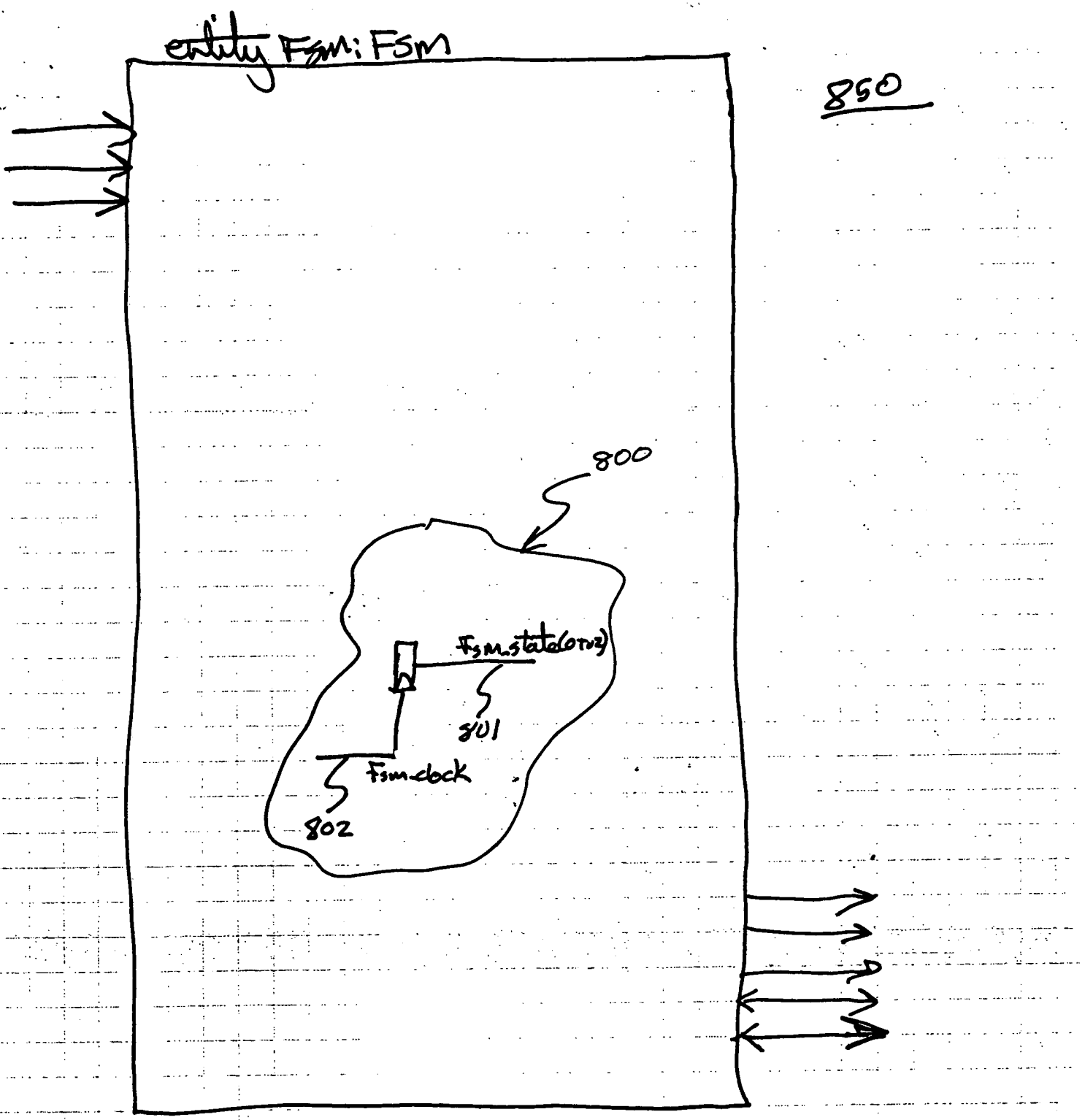


FIG. 8B (Amended)
(Prior Art)

```
entity Fsm IS
  PORT(
        .... ports for entity Fsm .....
      );

  ARCHITECTURE Fsm of Fsm IS

  BEGIN

        .... HDL code For Fsm and rest of the entity...

        fsm_state(0 to 2) <= ... signal 801 ....

853 {   --!! Embedded Fsm : exampleFsm;                          } 852
859 {   --!! clock        : (fsm_clock);                         }
854 {   --!! state_vector : (fsm_state(0 to 2));                 }
855 {   --!! states       : (s0, s1, s2, s3, s4);                }
856 {   --!! state_encoding : ('000', '001', '010', '011', '100'); }
857 {   --!! arcs         : (s0=>s0, s0=>s1, s0=>s2,             }
    {   --!!                s1=>s2, s1=>s3, s2=>s2,             }
    {   --!!                s2=>s3, s3=>s4, s4=>s0);            }
858 {   --!! end Fsm;

  END;
```

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FIG. 8C (Amended)